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Abstract
The design of VLSI has into SOC（system-on-chip）era, many different functions are integrated into a single chip. Full adders is usually adopted in the arithmetic logic unit of a digital system, e.g. ALU inside a CPU, many kinds of ASIC（Application Specific Integrated Circuit）chips, and various of cryptographic systems. If we can refine the architecture of a full adder, the performance of a chip using the refined full adder will be increased. Many different architectures of a full adder were proposed, the structure of 10-T（10 transistors）full adder was a balanced design regarding transistor counts and performance. Thus, we try to design 10-T full adder in this thesis.
Six novel 10-T full adder structures are proposed in this thesis, The comparison between the proposed adders and the prior works was also performed. The proposed designs possess the advantages of better performance of power consumption and time delay. If will be a better alternative to use the proposed full adder architecture in a high speed as well as low power digital circuit.
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